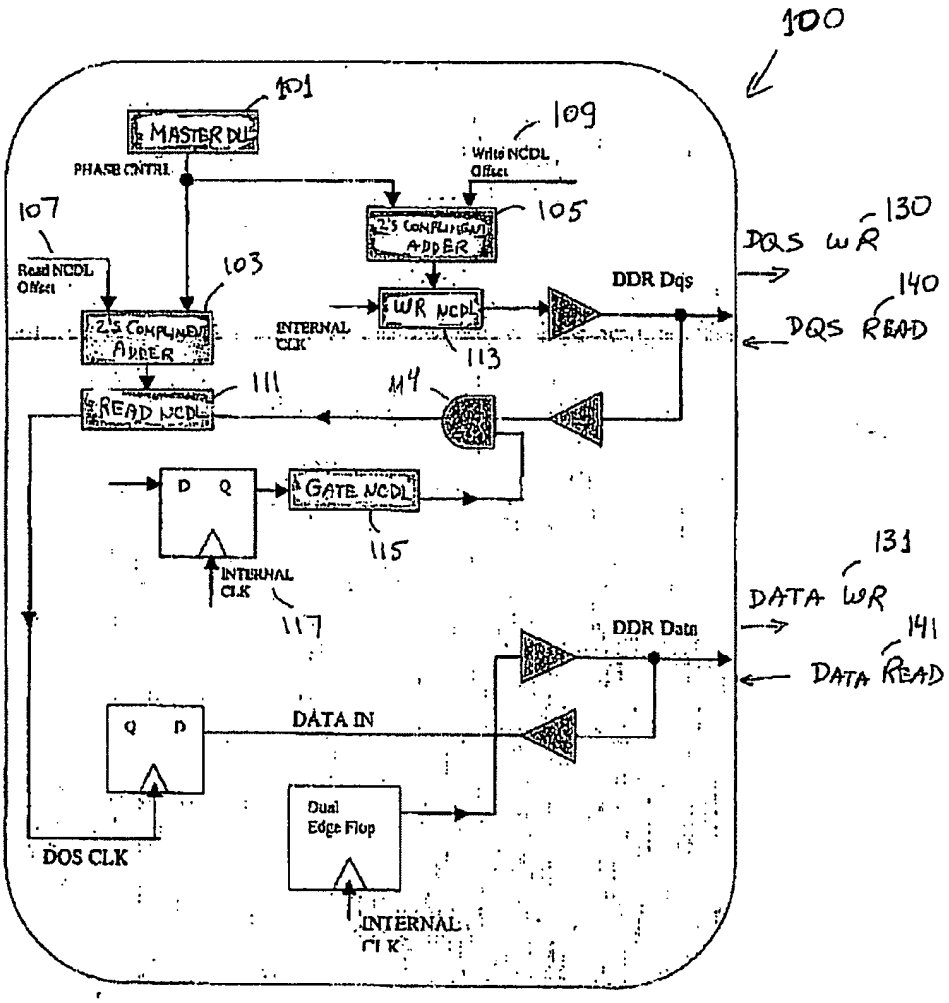

FIG. 1: DLL and NCDL mechanism in DDR memory controller

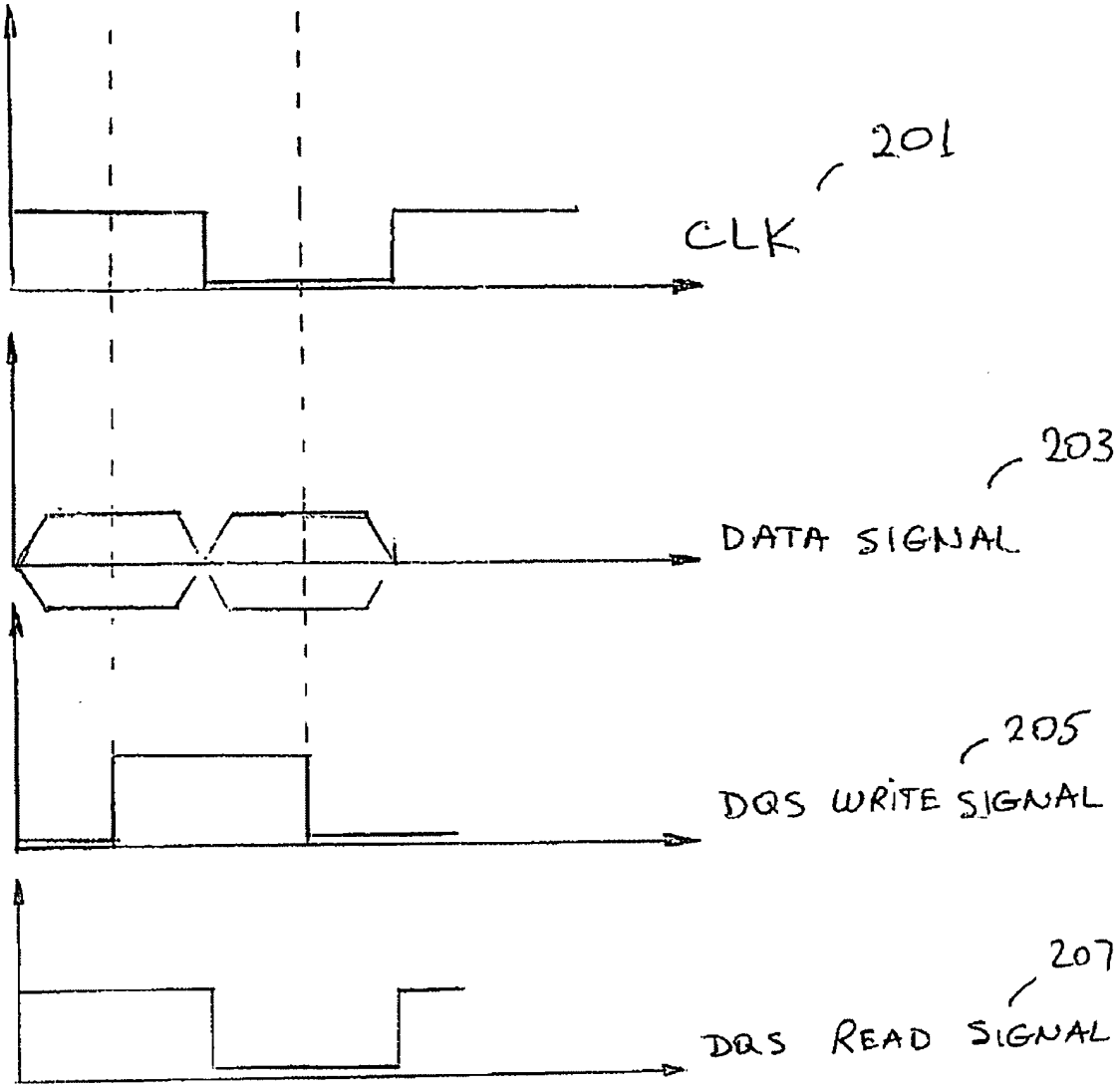

FIG. 2 : CENTER ALIGNMENT OF DQS SIGNAL AND DATA SIGNAL

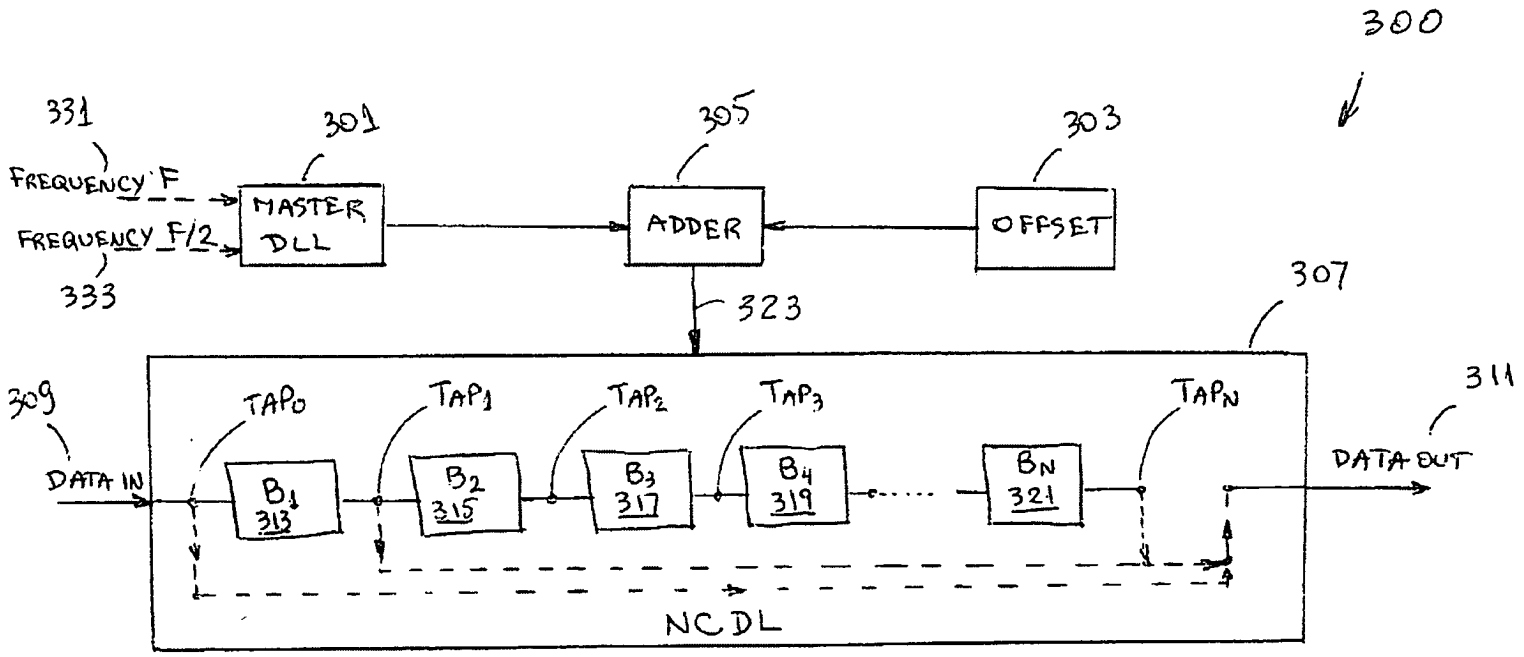

FIG. 3 : HARDWARE FOR SIGNAL DELAYING USING A NUMERICALLY CONTROLLED DELAY LINE

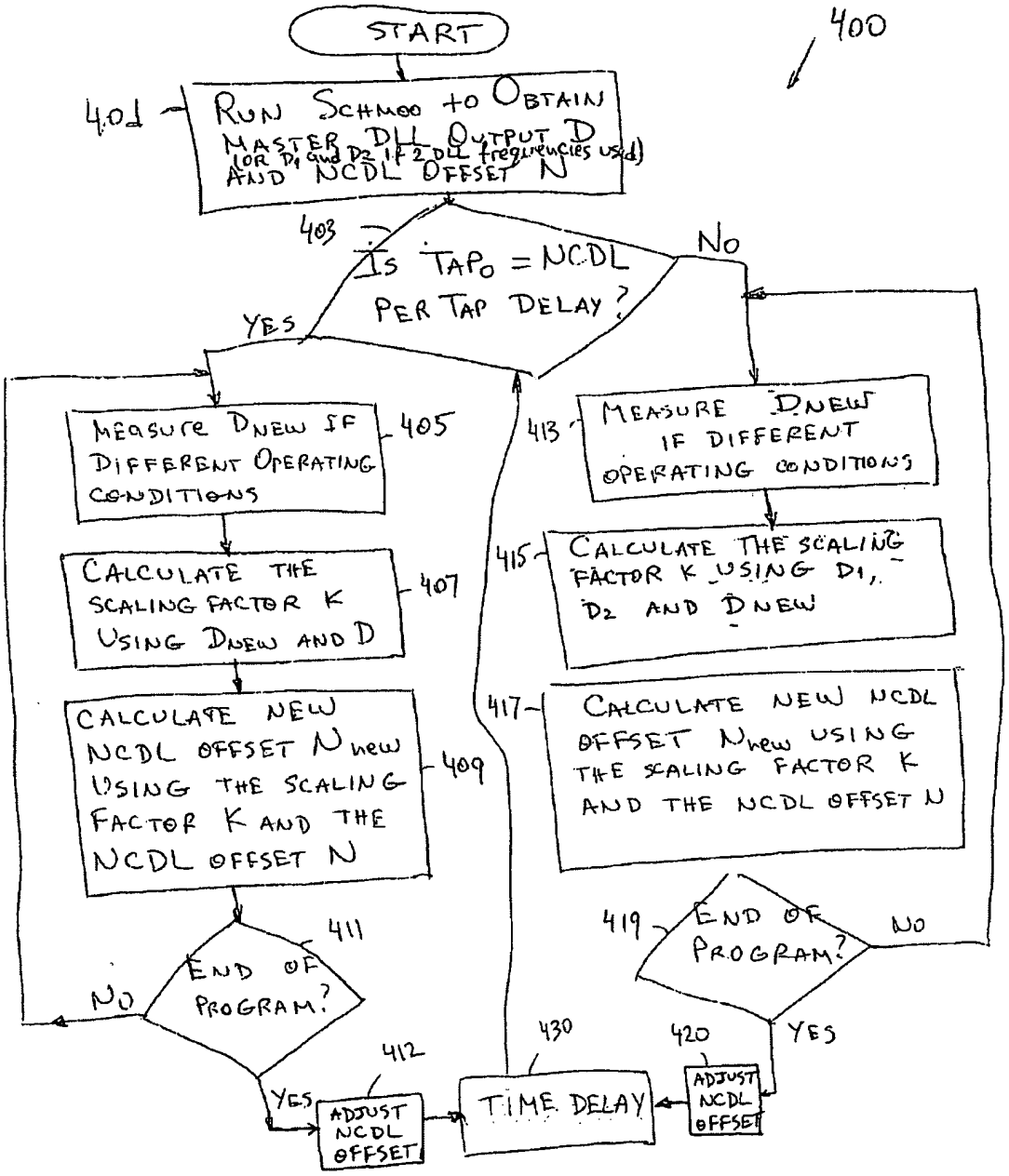

FIG. 4. METHOD FOR UPDATING AN NCDL OFFSET USING A SCALING FACTOR

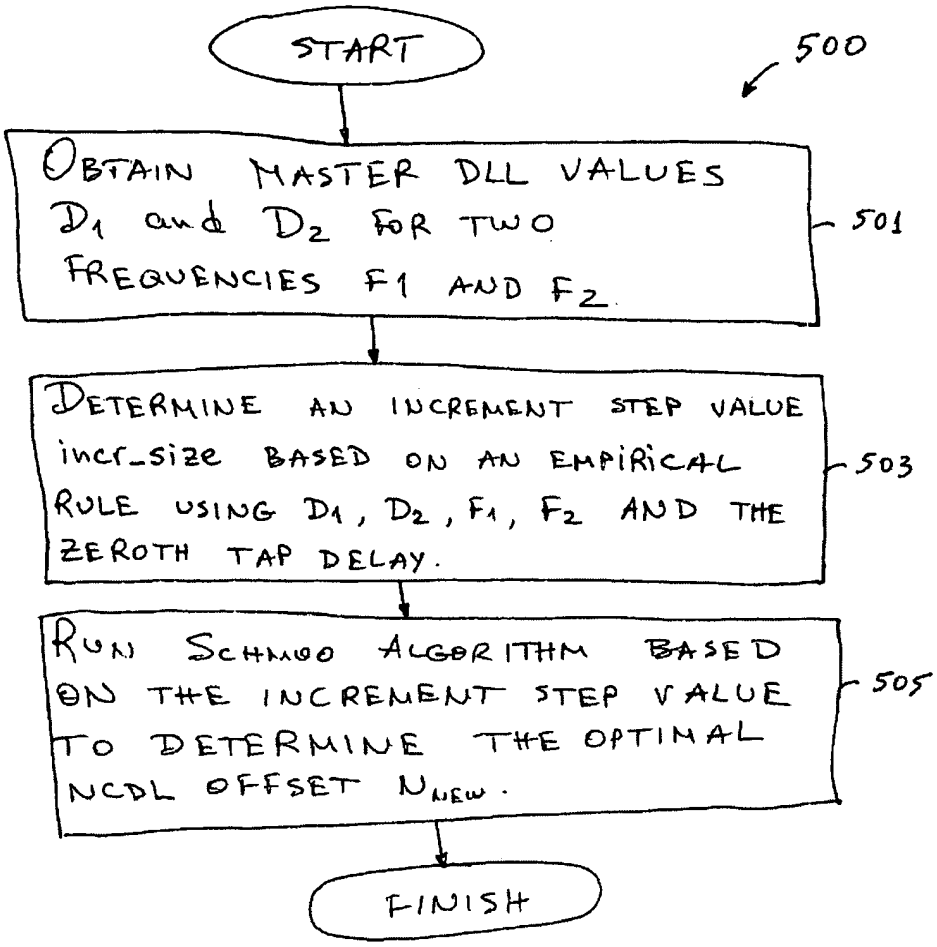

FIG. 5: METHOD FOR OPTIMIZING THE SCHMOO RUNTIME ALGORITHM BY DETERMINING AN INCREMENT STEP VALUE.

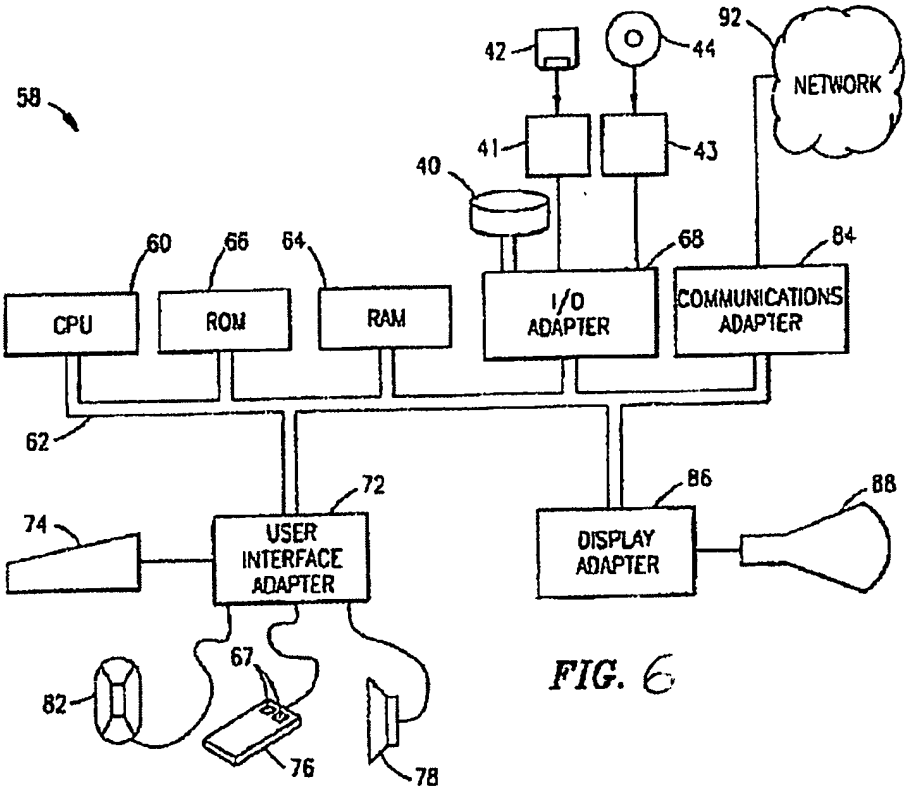

FIG. 6